CLAIMS

WE CLAIM:

1. A mapping circuit for vectors of Q-many bits, the circuit comprising:

n-many MUX's, $n \leq Q$, and each MUX having at least Q-many data inputs to which are coupled the Q-many bits of the vector to be mapped, the correspondence between the Q-many data inputs and the bits of the Q-bit vector to be mapped being the same for each MUX;

each MUX having an output bit that will represent the signal at one of the Q-many data inputs of that MUX;

each MUX also having a collection of at least m control inputs, $2^m \geq Q$, to which are coupled for each MUX a corresponding separate collection of control signals whose values indicate which of the Q-many data inputs will have its signal coupled to the output bit;

the output bits for the n-many MUX's forming an ordered collection of signals constituting a mapped vector according to a mapping defined by the n-may collections of m-many control signals;

a memory having an address and containing addressable locations each storing the values of the m-many control signals for the n-many MUX's and also having data outputs coupling those control signal values to the control inputs of their respective MUX's; and

a programmatically controlled address applied to the memory and that selects the mapping to be used to map the vector.

2. A circuit as in claim 1 wherein $n = Q$ and the vector is transmitted to a device under test.

3. A circuit as in claim 1 wherein $n<Q$ and the vector is comparison results between a desired response and an actual response for a device under test.